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LIU, LI	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,365	COFFEY, JOSEPH	
	Examiner	Art Unit	
	Li Liu	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *05 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on March 05, 2007 with respect to claims 1, 14 and 16 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments with respect to claims 2, 7 and 15 have been fully considered but they are not persuasive. The examiner has thoroughly reviewed Applicant's amendment and arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

1). Applicant's argument – "Independent claim 7 requires that the 'electrical to electrical cards each including a rear interface portion for mating with the electrical interface port', the electrical interface port found on one of the plurality of optical to electrical cards. ... Choy et al does not disclose or suggest direct connection between an electrical to electrical card and an optical to electrical card".

Examiner's response – As shown in Figures 2, 3 and 4, Choy et al discloses a plurality of electrical to electrical cards (14 in Figure 2 and 4, column 6 line 62-column 7 line 12) each including a rear interface portion (42 and 44 in Figure 2) for mating with the electrical interface port of the optical to electrical card via the backplane connectors (column 7 line 13-22). The claim 7 does not disclose a **direct** connection between an electrical to electrical card and an optical to electrical card.

2). Applicant's argument – "Regarding claim 2, ... Choy et al teaches cost reduction by minimizing the number of components and fiber links incorporated into a system. Specifically, Choy et al states that 'As the number of different types of data

communications equipment increases, it can be appreciated that the expense associated with renting additional fiber pairs may become prohibitive.' Therefore, Choy et al teaches away from use of extra fiber pairs, even for redundancy and error correction".

Examiner's response – The above mentioned problem is discussed in the Background of the Invention for conventional multiplexing equipment, especially for users using different equipments and different communication protocols (column 1, line 54-67). Choy actually solves the mentioned problem, "The foregoing and other problems are overcome by wavelength division multiplex communications apparatus that is constructed in accordance with the invention, and by a method of operating same." (column 2, line 3-5). Choy et al never state that an additional fiber cannot be used as a protection fiber or error correction.

3). Applicant's argument – "Regarding claim 15, Applicant first notes that the Examiner has provided no motivation to use the NRZI format, because there is no indication in Choy et al itself that the NZRI format would be particularly desirable".

Examiner's response – As admitted by the applicant, the NRZI is just one of the common format signals. The NRZI has been widely used in the communications since it is especially helpful in situations where bit stuffing is employed -- the practice of adding bits to a data stream so it conforms with communications protocols. Choy et al's system is fully operable to use NRZI because "[t]he provision of the General Purpose interface provides an open (protocol independent) capability" (column 5, line 1-13).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Choy et al (US 5,487,120).

1). With regard to claim 7, Choy et al discloses a WDM chassis comprising:

a backplane (Figure 4), including an input power port, a control signal port, and a plurality of optical interface ports for interfacing with an optical to electrical conversion card, each optical interface port including a power port, a control signal port, and at least one optical port (column 7 line 13-22);

a plurality of optical to electrical cards (20 in Figure 3A and 4) each including a backplane interface portion (53 and 54 in Figure 3A connected via BACKPLANE) for mating with the optical interface port and including a power port, a control signal port (Laser Control Status, Received Data Status, column 7 line 20-21), and at least one optical port (53 and 54 in Figure 3A, and I/O Fibers in Figure 4, column 6 line 40-44), each optical to electrical card (20 in Figure 4) including optical to electrical conversion circuitry for converting between common format signals and optical signals (Figure 3A), each optical to electrical card including an electrical interface port (52 and 64 etc in Figure 3A) including a power port, a control signal port, and at least one electrical port (Figure 3A, column 5 line 35 to column 6 line 18);

a plurality of electrical to electrical cards (14 in Figure 2 and 4, column 6 line 62-column 7 line 12) each including a rear interface portion (42 and 44 in Figure 2) for mating with the electrical interface port and including a power port (column 7 line 13-22, two converters are mated via the backplane connectors), a control signal port (PORT STATUS OUPUT in Figure 2), and at least one electrical port (42 and 44 in Figure 2), each electrical to electrical card including electrical to electrical conversion circuitry for converting between native protocol media signals and common format signals (30 and 32 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 35-39), each electrical to electrical card including a media interface port including at least one main signal port (column 7 line 13-22).

2). With regard to claim 8, Choy et al discloses wherein the at least one main signal port is a coaxial port (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

3). With regard to claim 9, Choy et al discloses wherein the at least one main signal port is a twisted pair port (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

4). With regard to claim 10, Choy et al discloses wherein the at least one main signal port is an optical port (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

5). With regard to claim 11, Choy et al discloses wherein the backplane defines a first plane (Figure 4), and the optical to electrical cards each define a second plane (20

in Figure 4) transverse to the first plane (the LRCs are plugged into a slot in the lower row, column 6 line 31 to column 7 line 12).

6). With regard to claim 12, Choy et al discloses wherein the electrical to electrical cards (14 in Figure 4) each define a third plane parallel to the second plane (IOC and LRC are parallel in Figure 4).

7). With regard to claim 13, Choy et al discloses the WDM chassis further comprising a chassis housing (66 in Figure 4) wherein the backplane defines a rear of the chassis housing, wherein the optical to electrical cards and the electrical to electrical cards are received in a front opening of the chassis housing (Figure 4, the IOC and LRC are displaced in front, column 6 line 36-50).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choy et al (US 5,487,120) in view of Sekiguchi (US 6,814,546).

1). With regard to claim 1, Choy et al discloses a WDM optical system comprising:

first and second WDM's (12a and 12b in Figure 1 and Figure 6);

an optical link (28 in Figure 1 and 6) for transmit and receive signals for each WDM; each WDM including circuitry including a multiplexer (24a in Figure 1 and 25a in Figure 6) and a demultiplexer (24b in Figure 1 and 24a in Figure 6);

each WDM including a plurality of separate optical to electrical converters (LRC 20 in Fiuger 1 and 6) each at a separate wavelength removably mated with the circuitry (pluggable module, column 6 line 62-64);

each WDM including a plurality of separate electrical to electrical converters (14 in Figure 1 and 6), each mated with one of the optical to electrical converters (42 and 44 in Figure 2, connected to LRC via BACKPLANE), each electrical to electrical converter including input and output signal locations (16a in Figure 1 and 6, column 4, line 14-17).

But, Choy et al does not disclose that the electrical to electrical converters is mated with one of the optical to electrical converters at a card edge connector.

Although Choy et al doesn't specifically disclose the card edge connector, such limitation is merely a matter of design choice and would have been obvious in the system of Choy et al. Choy et al teaches that the two converters are connected via a backplane connectors; that is the two converters are connected at a connector - the backplane connector. The limitations in claim 1 do not define a patentably distinct invention over that in Choy et al since both the invention as a whole and Choy et al are directed to a WDM system and use the electrical to electrical converters and optical to electrical converters. Therefore, how to connect the two converters would have been a matter of obvious design choice to one of ordinary skill in the art.

And another prior art, Sekiguchi discloses a card edge connector (13 and 14 in Figure 12), which is used to for external tester. The arrangement of the card edge connector improves the testing efficiency because inserting the card edge connector into the mating connector suffices to make a test.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a card edge connector as taught by Sekiguchi so that the electrical to electrical converters and optical to electrical converters are directly connected via a card edge connector, and the system can be made more compact and the diagnosis of devices can be made more convenient.

2). With regard to claim 3, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 1 above. And Choy et al further disclose wherein the circuitry includes a backplane (Figure 4) including two optical ports (two port of the BACKPLANE are used to connect to 53 and 54 in Figure 3A) for removably connecting to the separate optical to electrical converters.

3). With regard to claim 4, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 1 above. And Choy et al further disclose wherein the electrical to electrical converter converts coaxial signals into a common format electrical signal (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

4). With regard to claim 5, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 1 above. And Choy et al further disclose wherein the electrical to electrical converter converts twisted pair signals into a common format

electrical signal (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

5). With regard to claim 6, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 1 above. And Choy et al further disclose wherein the electrical to electrical converter converts optical signals into a common format electrical signal (30 and 32 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

6). With regard to claim 14, Choy et al discloses a WDM optical system comprising:

a first WDM (12a in Figure 1 and 6) including a chassis (Figure 4) and circuitry including a multiplexer (24a in Figure 1 or 25a in Figure 6);

a second WDM (12b in Figure 1 and 6) including a chassis (Figure 4) and circuitry including a demultiplexer (24b in Figure 1 or 25b in Figure 6);

an optical link (28 in Figure 1 and 6) for transmitting multiplexed optical signals from the first WDM for receipt by the second WDM;

each WDM including a plurality of separate optical to electrical converter cards (20 in Figure 1 and 6) received by each chassis, each optical to electrical converter card at a separate wavelength (Figure 3a, column 5 line 47-65) and removably mated with the circuitry (pluggable module, column 6 line 62-64);

each WDM including a plurality of separate main signal to electrical converter cards (14 in Figure 1 and 6) received by each chassis, each main signal to electrical converter card mated with one of the optical to electrical converter cards (42 and 44 in

Figure 2), each main signal to electrical converter card including a main signal port (30 in Figure 2).

But, Choy et al does not disclose that the electrical to electrical converters is mated with one of the optical to electrical converters at a card edge connector.

Although Choy et al doesn't specifically disclose the card edge connector, such limitation is merely a matter of design choice and would have been obvious in the system of Choy et al. Choy et al teaches that the two converters are connected via a backplane connectors; that is the two converters are connected at a connector - the backplane connector. The limitations in claim 1 do not define a patentably distinct invention over that in Choy et al since both the invention as a whole and Choy et al are directed to a WDM system and use the electrical to electrical converters and optical to electrical converters. Therefore, how to connect the two converters would have been a matter of obvious design choice to one of ordinary skill in the art.

And another prior art, Sekiguchi discloses a card edge connector (13 and 14 in Figure 12), which is used to for external tester. The arrangement of the card edge connector improves the testing efficiency because inserting the card edge connector into the mating connector suffices to make a test.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a card edge connector as taught by Sekiguchi so that the electrical to electrical converters and optical to electrical converters are directly connected via a card edge connector, and the system can be made more compact and the diagnosis of devices can be made more convenient.

7). With regard to claim 15, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 14 above. And Choy et al further discloses wherein the main signal to electrical converter cards convert between one of coaxial, twisted pair, and optical signals, and specific format electrical signals (column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39), wherein the optical to electrical converter cards convert between the specific format electric signals and optical signals at one of a selected wavelength for respective multiplexing and demultiplexing by the respective multiplexer and demultiplexer of the first and second WDM's (column 5 line 47 to column 6 line 30).

But, Choy et al does not expressly state that the specific format electric signal is the non return to zero inverted (NRZI) electrical signal. As admitted by the applicant, the NRZI is just one of the common format signals. The NRZI is a method of mapping a binary signal to a physical signal for transmission over some transmission media so that it keeps the sending and receiving clocks synchronized. The NRZI has been widely used in the communications since it is especially helpful in situations where bit stuffing is employed -- the practice of adding bits to a data stream so it conforms with communications protocols. Although Choy et al does not expressly disclose the NRZI, such limitation are merely a matter of design choice and would have been obvious in the system of Choy et al. Choy et al's system is fully capable of using NRZI because "[t]he provision of the General Purpose interface provides an open (protocol independent) capability". The limitations in claim 15 do not define a patentably distinct invention over that in Choy et al since both the invention as a whole and Choy are

directed to provide a protocol independent capability and support a large variety of serial data stream types. Therefore, to use NRZI or other type electrical signals would have been a matter of obvious design choice to one of ordinary skill in the art.

8). With regard to claim 16, Choy et al discloses a method of optical system management comprising:

providing multiplexing and demultiplexing circuitry (24 in Figure 1 and 24 and 25 in Figure 6) for a multi-channel signal system;

mating a plurality of optical to electrical converter cards to the circuitry (22 in Figure 1 and 6, 53 and 54 in Figure 3A), each optical to electrical converter card selected to transmit and receive optical signals at a distinct wavelength of light relative to the other optical to electrical converter cards of the multi-channel system (Figure 3a, column 5 line 47-65);

mating an electrical to electrical converter card to a selected one of the optical to electrical converter cards (18 in Figure 1 and 6, 42 and 44 in Figure 2), wherein the electrical to electrical converter card transmits and receives native protocol media signals in a first format, and converts the signals to a second electrical format (Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39), wherein the signals of the second electrical format are converted to optical signals at the distinct wavelength of light of the selected optical to electrical converter card (Figure 3a, column 5 line 47-65).

But, Choy et al does not disclose that the electrical to electrical converters is mated with one of the optical to electrical converters at a card edge connector.

Although Choy et al doesn't specifically disclose the card edge connector, such limitation is merely a matter of design choice and would have been obvious in the system of Choy et al. Choy et al teaches that the two converters are connected via a backplane connectors; that is the two converters are connected at a connector - the backplane connector. The limitations in claim 1 do not define a patentably distinct invention over that in Choy et al since both the invention as a whole and Choy et al are directed to a WDM system and use the electrical to electrical converters and optical to electrical converters. Therefore, how to connect the two converters would have been a matter of obvious design choice to one of ordinary skill in the art.

And another prior art, Sekiguchi discloses a card edge connector (13 and 14 in Figure 12), which is used to for external tester. The arrangement of the card edge connector improves the testing efficiency because inserting the card edge connector into the mating connector suffices to make a test.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a card edge connector as taught by Sekiguchi so that the electrical to electrical converters and optical to electrical converters are directly connected via a card edge connector, and the system can be made more compact and the diagnosis of devices can be made more convenient.

9). With regard to claim 17, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 16 above. And Choy et al further disclose wherein the electrical to electrical converter card transmits and receives a coaxial native protocol

media signal (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

10). With regard to claim 18, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 16 above. And Choy et al further disclose wherein the electrical to electrical converter card transmits and receives a twisted pair native protocol media signal (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

11). With regard to claim 19, Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 16 above. And Choy et al further disclose wherein the electrical to electrical converter card transmits and receives an optical native protocol media signal (30 in Figure 2, column 4 line 14-17, and line 43-59, and column 5 line 1-13 and line 35-39).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choy et al (US 5,487,120) and Sekiguchi (US 6,814,546) as applied to claim 1 above, and in further view of Ramaswami et al (US 6,571,030).

Choy et al and Sekiguchi disclose all of the subject matter as applied to claim 1 above. But Choy et al does not expressly disclose the WDM optical system further comprising splitter circuitry, wherein the optical link includes dual optical links, wherein two transmit and two receive signal pathways are provided.

However, the redundant 1+1 protection has been widely used in the optical communications for providing extremely rapid recovery from network/path failure.

Ramaswami et al discloses one of these protection schemes (Figure 12, column 11, Section IV).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the splitter to create two optical paths so that a fast restoration or recovery of signals can be obtained and the system reliability is increased.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dallesasse et al (US 2005/0084269) discloses a modular optical transceiver for use in an optical WDM transmission system.

Lange et al (US 6,944,404) discloses a WDM network transceiver.

Owens et al (US 2003/0169566) discloses a WDM add/drop multiplexer module.

Bhalla et al (US 6,915,036) discloses a field reconfigurable line cards for an optical transport system.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li Liu whose telephone number is (571)270-1084. The examiner can normally be reached on Mon-Fri, 8:00 am - 5:30 pm, alternating Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571)272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Li Liu
May 21, 2007

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER